Principles and Practices: Multisim in Teaching Digital Systems Design

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1. INTRODUCTION

Digital hardware plays a dominant role in many electrical and computer engineering products today. The introductory course Digital System Design is a core requirement course for electrical and computer engineering students. Integrating HDL (Hardware Description Language), such as Verilog or VHDL into the teaching of logic system design has been proposed in the past (Areibi, 2001; Chang, 1997; Pedraza-Chavez, *et al.*, 1995; Reid, 2000; Roth, 1994). However, for the early introduction of HDL, the instructor has to focus on explaining the important differences between HDL and other computer programming languages that students are familiar with. Students may focus upon the complex features of HDL instead of the fundamentals and principles of logic systems. If HDL is introduced at the same time as the logic system, then it is a big distraction from the teaching of these fundamental principles and practices of digital logic systems. These basic principles include Boolean algebra, Karnaugh maps, synchronous and asynchronous sequential circuits, to name a few. Because the schematic concepts and the digital logic blocks are the blueprints of digital logic systems, thus it is very necessary to help students learn the basic principles first instead of jumping to VHDL directly. While it is agreed that students must learn about these digital logic functions and their implementations, whether to introduce HDL language too early into the teaching of digital system designs remains a controversy. Teaching digital systems design using hands-on experience on breadboards and Xilinx FPGA was proposed by us (Wang, 2005), the author's experience showed that this approach is very effective to let students exposed to both principles and practices of digital systems.

This paper presented our experience of using Multisim (Multisim, 2005) schematic capture simulation tools together with the hands-on breadboard techniques in the lab sessions. It has been shown that through the Multisim high-level simulation, students can better understand the principles and they can evaluate their designs quickly. By the hand-on experiences on the breadboards, the experiences of design and practices can be strengthened. This will help students develop the practical techniques of design, troubleshooting and implementation skills for the digital systems.

ECE 270 – Introduction to Digital System Design is a core course offered every semester. This course extends over fourteen weeks with three hours of lectures per week and thirteen laboratory sessions. Topics include combinational circuits (such as decoder, encoder, arithmetic functions, multiplexers) and sequential circuits (such as latches, flip-flops, counter, shift registers and sequential state machines). The main purposes of this course are (1) to teach students the basic

concepts and functional blocks in digital logic design and (2) to illustrate the design and implementation procedure of digital logic systems (3) to troubleshoot and debug the digital logic systems from hands-on lab exercises. Extensive examples are introduced throughout this course. The different radix representations are introduced first, followed by logic gates, static and dynamic characteristics, Boolean algebra, Karnaugh maps, combinational circuit analysis and practices, sequential circuit analysis and practices, with sequential state machines introduced in the end. The textbook "Digital Electronics: A Practical Approach" (Kleitz, 2005) is adopted for this class.

The lab exercises are based on five experiments using breadboard, eight lab sessions using Xilinx ISE schematic capture, Modelsim simulation and XSA-100 FPGA/CPLD boards. In the first five labs, the practices of bread-board together with Multisim, students learn the debugging and troubleshooting techniques in the implementation and verification of digital systems. In the schematic design, simulation and verification using Xilinx ISE and FPGA/CPLD boards, students focus on the learning of logic block functions and the design of a moderately complex digital system using these digital logic blocks.

2. MULTISIM INTRODUCTION

Currently, embedded microprocessor and Programmable Logic Devices (PLD) such as FPGA, CPLD are the primary components in modern digital systems. The use of PLDs allow the user to download the design and replaces the former part of interconnected fixed-function MSI TTL or CMOS chips. However, the functions and applications of the traditional 74 series TTL are explained in most current available textbooks and the 74-series TTL chips find the major market in the university labs. In the lab sessions with breadboards, students also need to get the pinout diagram in order to wire them. It will take the student significant time (nearly 2 hours) to wire the breadboard which leaves them little time to learn about how the circuit works.

Multisim is a complete system design tool that offers a very large component database, schematic entry, full analog/digital SPICE simulation, VHDL/Verilog HDL design entry and simulation, FPGA/CPLD synthesis, RF capabilities, post-processing features and seamless transfer to PCB layout packages such as Ultiboard. It offers the full capability of capture, simulation and analysis of the electronic schematic circuits. After the schematic design is captured, Multisim provides you with an interactive oscilloscope, bode plotter, logic analyzer, power supply, multimeter, function generator, etc to simulate and analyze the design. With Multisim, the student's opportunities are expanded to allow them to try new situations and analyze the results that they have learned to foresee through the theories and principles. The adoption of Multisim in the teaching of digital systems design course at IPFW (Indiana-Purdue University Fort Wayne), it never intends to substitute for the hands-on experimentation on the breadboards, on the other hand, it allows the students to get the pre-knowledge of the oncoming lab sessions. Besides, many students discovered that the IC libraries in MultiSim® provide pinout diagrams, and they call these up to help them wire the corresponding hardware ICs.

Currently in the ECE 270 lab sessions, Multisim is used for the first five labs and they are presented in the following laboratory activities:

3. LABORATORY ACTIVITIES

3.1 Lab 1: Introduction to Digital Logic Devices

This is the first lab session. The main objective of this lab is to introduce the students to simple digital devices and their operations. They will also be introduced to the procedure of building simple digital circuits using a digital design kit. Some students don't touch any breadboard and electronic components before this lab and so they have no knowledge of what will happen in the oncoming lab practices. Multisim gives them a good starting point to see what they are going to encounter and what they are going to do. The simulation of the simple AND, OR and Inverter testing circuit are required to be performed before the lab. A testing logic circuit for the inverter 74LS04 is shown as Figure 1. In the simulation, the LED output of the inverter can be turn on/off through a specific key press on/off on the keyboard, thus before the lab session, students already have some knowledge.

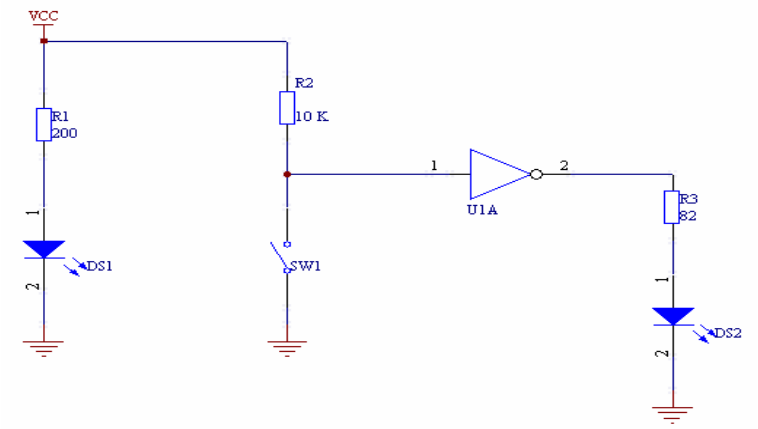

Figure 1. 74LS04 Testing Circuit in Lab 1

3.2 Lab 2: Timing Diagram

The main objective of this lab is to learn to use function generator and oscilloscope to display the timing diagram of basic logic gates. Students will also know how to draw the timing diagram. These objectives can be facilitated by using Multisim simulation. A function generator and an oscilloscope will be connected to the testing circuit in the simulation and the input/output timing diagrams are displayed on the oscilloscope screen, then the students will conduct the same procedure and practices on the breadboards. This approach greatly strengths the students' knowledge of principles and practices. Figure 2 shows a testing circuit used in Lab 2. Figure 3 is the timing diagram of the input/output waveforms when the switch is pressed on and the input signal is disabled. Figure 4 is the timing diagram of the input/output waveforms when the switch is released and the input signal is enabled to the output.

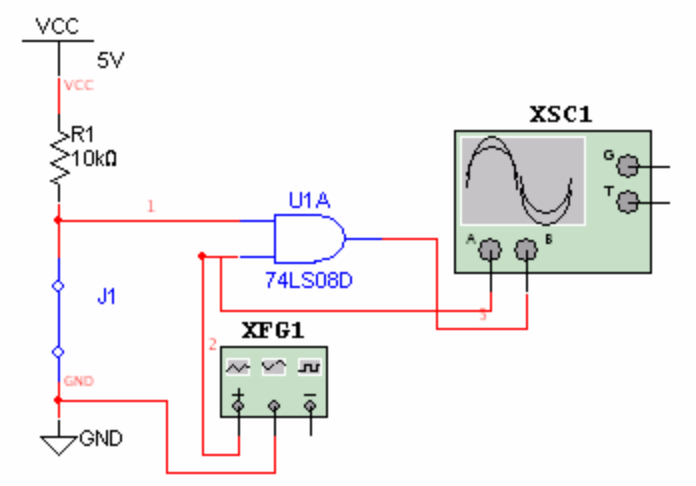

Figure 2. Timing Diagram Logic Circuit in Lab 2

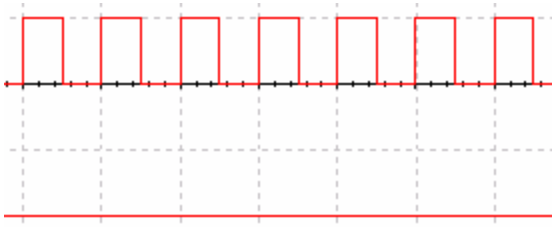

Figure 3. Timing Diagram with Switch On

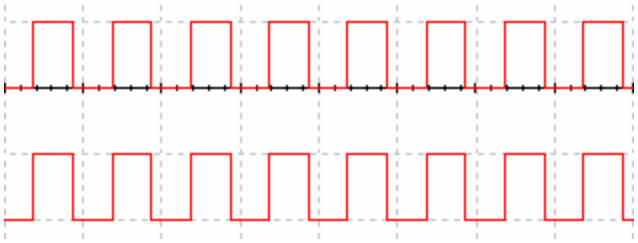

Figure 4. Timing Diagram with Switch Off

3.3 Lab 3: Implementation of a Logic Function

The main objective of this lab is to implement a simple logic function using 74-series ICs in different approaches. In part 1, only AND, OR and Inverter logic gates can be used. In part 2, only NAND gates can be used to realize the logic equation F(X,Y,Z)= X(Y'+Z) + X'Y.

Through this lab session, students will further understand the procedure of simulation, troubleshooting in the design procedure. A Multisim simulation of the design is required before the hands-on breadboard experimentations begin. Figure 5 shows the logic diagram in Multisim

using AND, OR and Inverter logic gates and Figure 6 is the logic diagram using only two-input NAND gates.

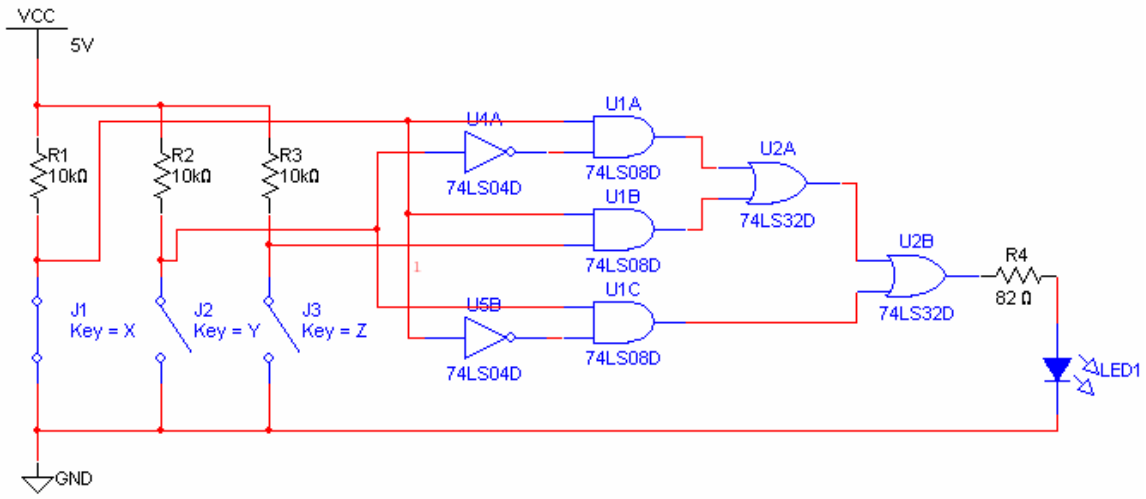

Figure 5. Logic Diagram using AND, OR and Inverters in Lab 3

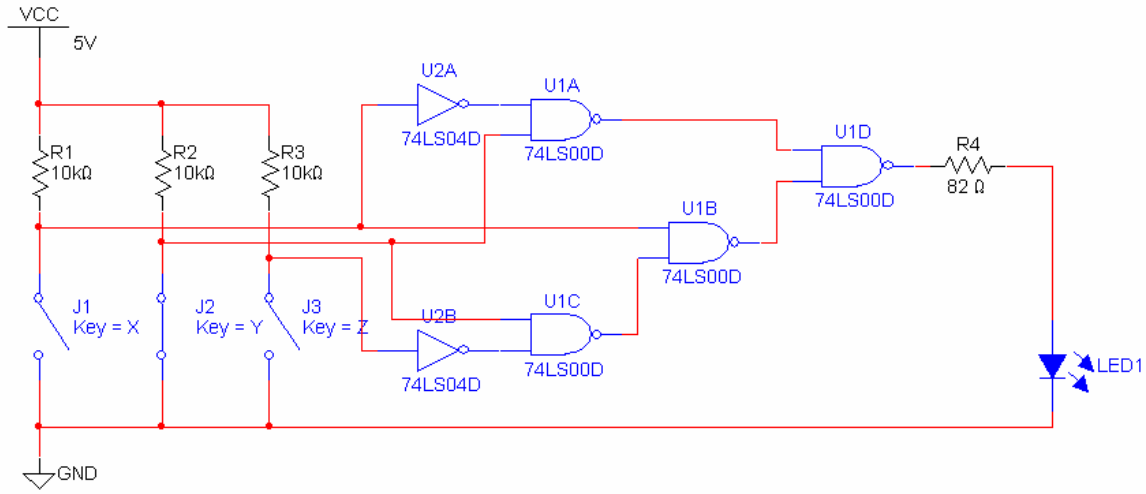

Figure 6. Logic Diagram using Only Two-input NAND Gates in Lab 3

3.4. Lab 4: Design of An Office Alarm System

In this lab, students will design a simple office alarm system using only NAND gates. This office alarm system requires a logic circuit that will trigger a camera to take a picture when any of the following conditions are met:

1. The office door is opened outside normal office hours
2. One of the desks is opened while the desk alarm is armed

Four sensor devices provide the following input signals:

DOOR	Low output (0V) from this sensor if the office door is open
ARMED	High output (5V) from this sensor if the desk alarm is armed
TIMER	High output (5V) from this sensor during normal office hours
DESK	Low output (0V) from this sensor if all desks are closed

One output signal controls the camera:

CAMERA	The camera takes a picture when CAMERA is low voltage (0V)

Before the lab session on the breadboards, students also need to design and simulate using Multisim. The captured schematic in Multisim can be used as blueprint in the oncoming lab session. A sample logic circuit for this design is shown as Figure 7.

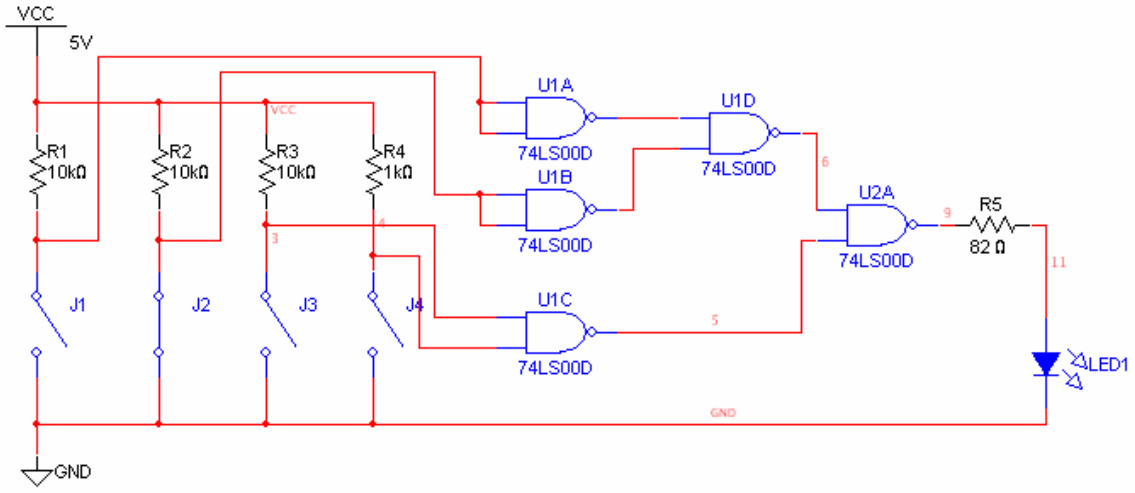

Figure 7. Logic Diagram of the Office Alarm System in Lab 4

3.5 Lab 5: Investigation of Timing Hazard

In this lab, students will learn what causes timing hazards in the combinational logic circuits, how hazards due to single input changes can be eliminated, and what happens if more than one input is allowed to change simultaneously. There are three parts in this lab and Multisim can be used for each part in the pre-lab preparations

- **Part 1:** Design and test the logic circuit for the logic equation: F=XZ'+YZ. In this part, students need to simulate and test their designs in Multisim and verify it on the breadboards. A sample of the schematic diagram is shown in Figure 8.

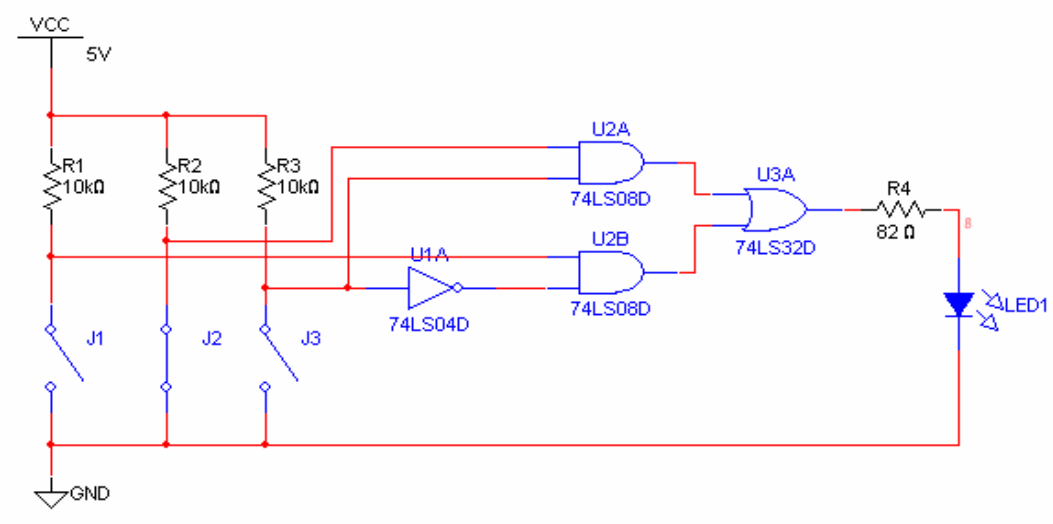

Figure 8. Logic Diagram of Timing Hazard in Lab 5 Part 1

- **Part 2:** After the functionality of the circuit has been verified in part 1, then X,Y are set as '1' and Z is set from the functional generator as 1Khz and 0-5V square waveform. The output waveform is being displayed on the oscilloscope screen. Figure 9 shows such a logic diagram. A timing hazard occurs and the simulation waveform is displayed on the oscilloscope as Figure 10.

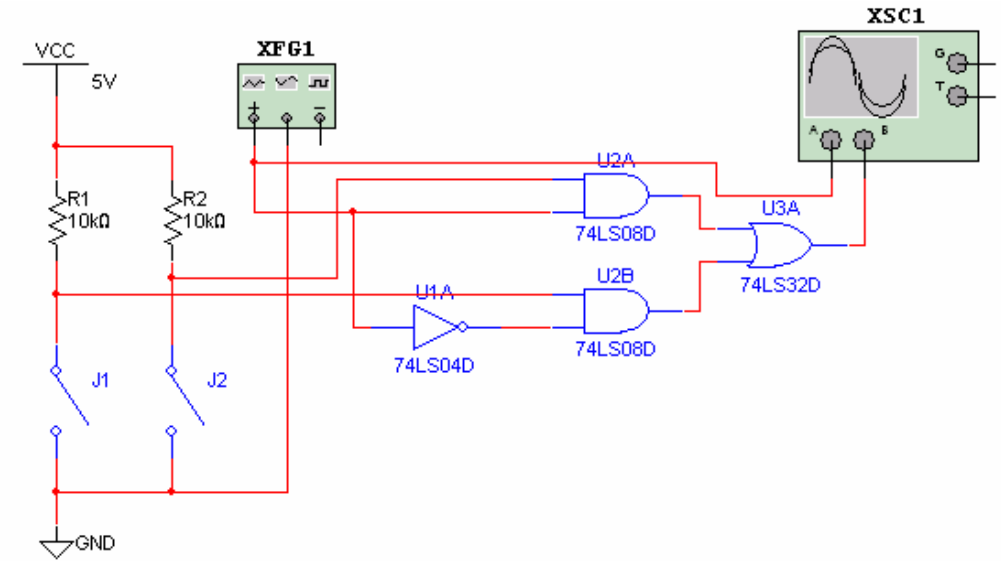

Figure 9. Logic Diagram of Timing Hazard in Lab 5 Part 2

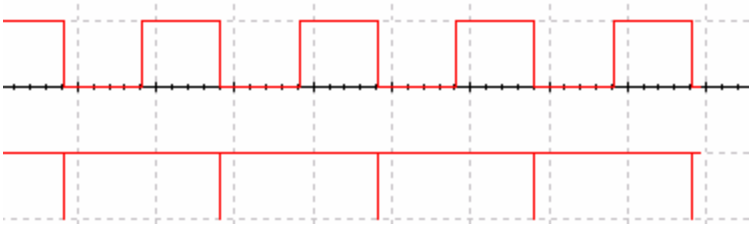

Figure 10. Simulation Waveform of Timing Hazard

- **Part 3:** The logic circuit in Part 2 is modified to eliminate the timing hazard with an extra AND gate is added as shown in Figure 11. A timing hazard-free simulation waveform is shown as Figure 12 using Multisim.

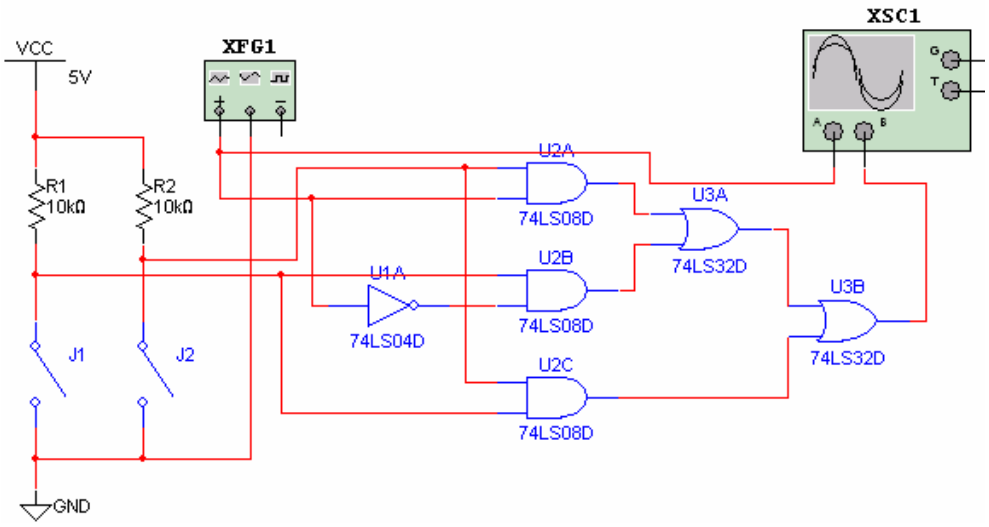

Figure 11. Timing Hazard-Free Logic Diagram in Lab 5 Part 3

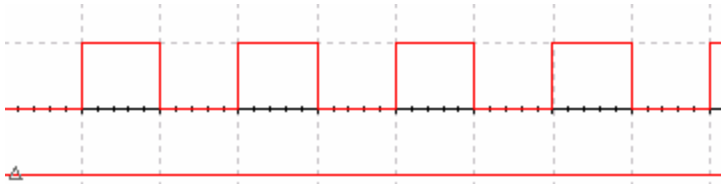

Figure 12. Simulation Waveform of the Timing Hazard Free Circuit

4. SUMMARY

In the teaching of digital systems design, the lab part is a very important and inseparable activity in the learning process. While the hands-on breadboard experimentations let students learn the techniques of debugging, wiring, troubleshooting, Multisim simulation is introduced to facilitate the students' learning. Through the Multisim high-level simulation, students can better understand the principles and they can evaluate their designs quickly. Our experience shows that this approach is very effective to let students exposed to both principles and practices of digital systems.

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