SOLAR ARRAY PEAK POWER TRACKER

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1. INTRODUCTION

Satellites in orbit above the Earth's atmosphere are powered by solar arrays. A challenge arises when a satellite will travel through intervals of darkness while in the Earth's shadow, knows as eclipses. A battery, the alternate power source during an eclipse, must be continuously recharged during each period of daylight by the solar array. The goal of the current solar array peak power tracker is to assure that the maximum power is transferred from the solar array to the satellite during the period of daylight (Button 1995). There are some constraints placed on this senior design project by the sponsor, NASA Lewis Research Center. It is their desire that the design be a stand-alone, digital solution. Other specifications are that the device must maintain a safe current level (approximately 10 amperes), include interfacing with power electronics and sensors, and must be able to be packaged in less than a four square inch board area. A series connected boost converter (SCBC) configuration must be used to generate the necessary voltage from the solar arrays.

2. SYSTEM DESIGN

Solar cells are known to be nonlinear. There exists one operating point for a given condition where the solar array produces maximum power. Figure 1 shows typical solar array current-voltage (I-V) and power-voltage (P-V) curves, which illustrate the main objective of the desired system. The voltage must be forced to stay near the maximum voltage point (V_{MP}). The goal of the system is to maintain a required voltage level to provide maximum power to the satellite power load, while continuously charging the battery with any excess power available from the solar array [Button 1996].

2.1 SCBC Configuration

The specified solar array is designed to generate an output voltage of 30 V. The supply voltage requirements on the satellite system are anticipated to be 42 V. Therefore, a Series Connected Boost Converter Configuration (SCBC) is used as shown in Figure 2 (Button 1999). The output of the system will be $V_{in}+V_{boost}$, where V_{in} is the output voltage of the solar array, and V_{boost} is the boost voltage obtained by the dc-dc converter.

The trim pin is used to adjust V_{boost} and will be controlled by the microcontroller to place the system at its maximum power transfer point.

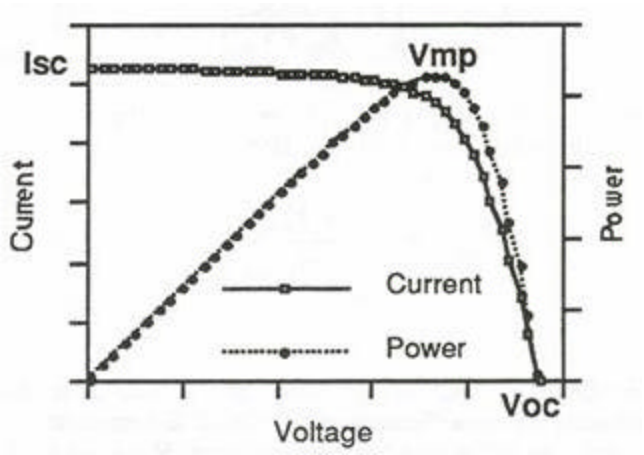

Figure 1. Power and current characteristics of a solar array

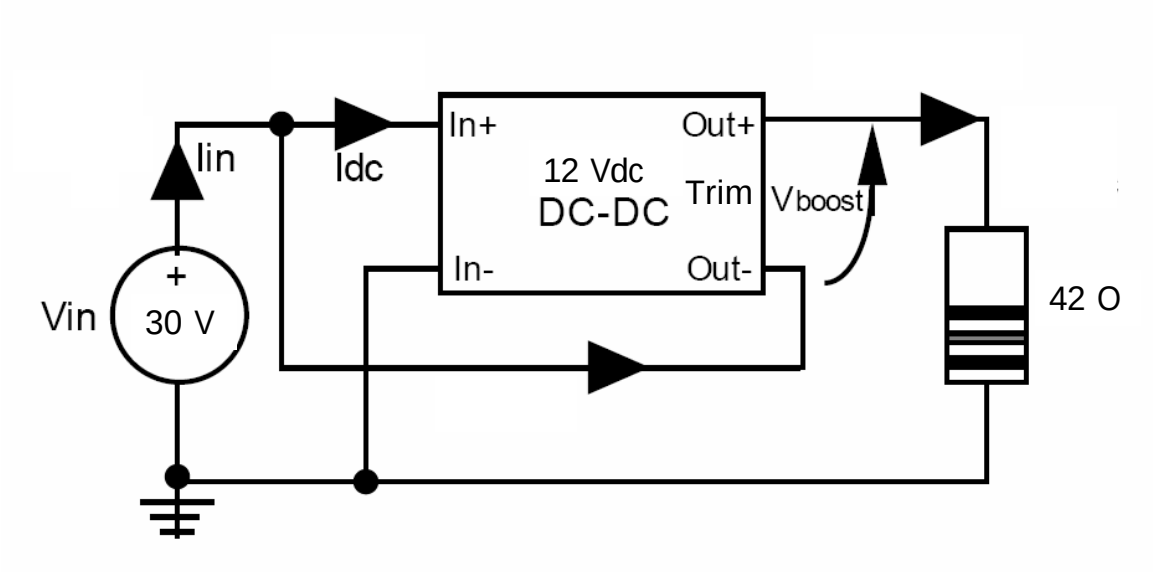

Figure 2. SCBC Configuration

2.2 Trim Control

The trim option of the DC-DC converter chip allows for the output voltage to be changed by a range of 6 to 13.2 volts (50-110%). This can be accomplished by converting the percent of the 24 possible volts desired to a percent of 5 volts allowable for the trim option. A table was created with conversion for the microcontroller to call upon within the algorithm, and is governed by the following equation:

$$V_{Tr} = \left(\frac{V_{inc}}{24} \right) \cdot 5 \qquad (1)$$

where V_{Tr} is the trim voltage that will need to be sent to the chip from the microcontroller and V_{inc} is the desired increase in voltage from the input voltage of the source. Therefore, to obtain a boost voltage of 12V, V_{Tr} must be set to 2.5 V.

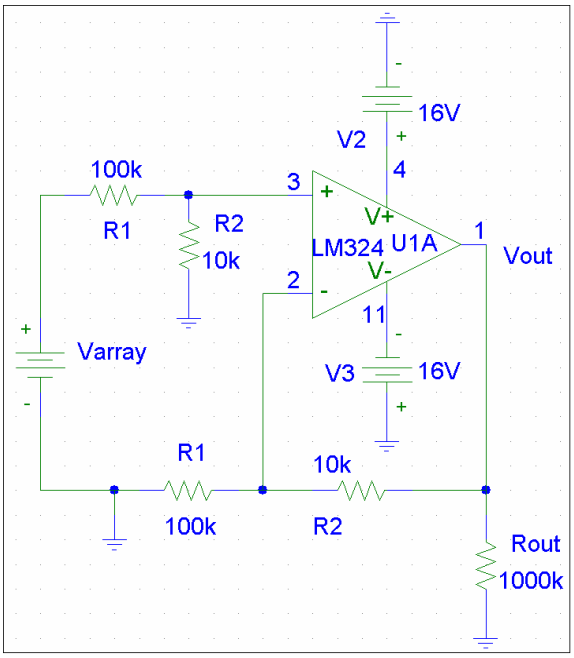

Figure 3. Voltage Sensing Circuit

2.3 Voltage Sensor

To sense the voltage supplied from the solar array, a differential op-amp circuit is designed. The voltage range of the solar array is too large to send to the processor directly and need to be stepped down. The circuit is set up to have a gain of 0.1. The circuit is shown in Figure 3. V_{OUT} will now have a range that is safe to send to the microcontroller for processing. We selected a LM324N op-amp because it has a larger input voltage range then a standard op-amp.

$$V_{OUT} = \frac{R_2}{R_1} \cdot V_{ARRAY} \quad (2)$$

$$V_{OUT} = \frac{10k}{100k} \cdot V_{ARRAY} \quad (3)$$

$$V_{OUT} = 0.1 \cdot V_{ARRAY} \quad (4)$$

2.4 Current Sensor

To sense the current supplied by the solar array simulator a LEM current transducer is used. This device uses the Hall Effect and therefore is isolated from the rest of the system. The sensor output supplies a current at 1/1000th of the sensed current. This current is converted to a sense voltage using a 100 Ω resistor. Thus the voltage

across the resistor will be $1/10^{th}$ of the sensed current and will be sent to the microcontroller.

$$I_{OUT} = \frac{I_{ARRAY}}{10} \tag{5}$$

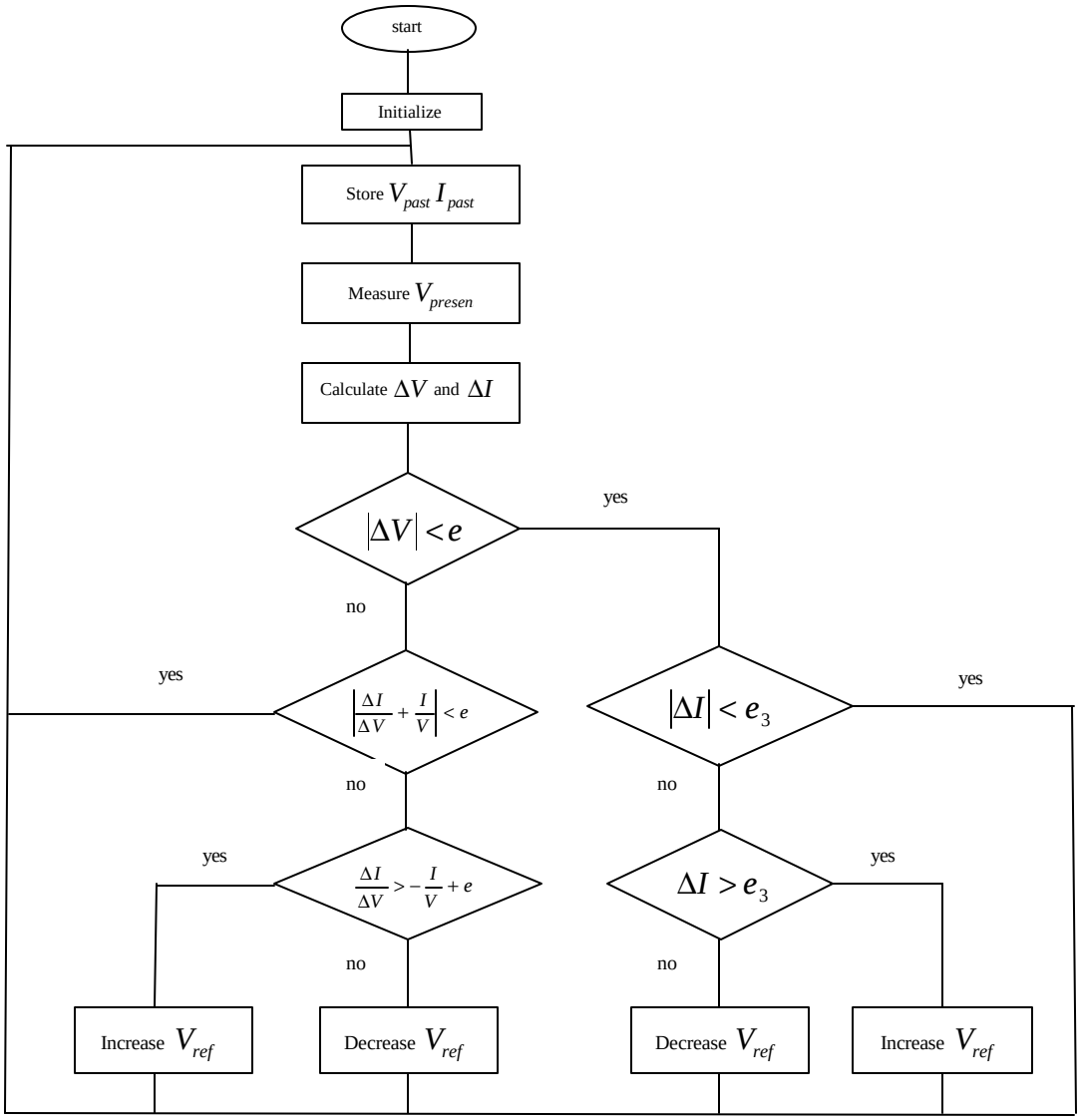

Figure 4. Flow chart of the search procedure.

2.5 Control Algorithm and its implementation

The algorithm that is used to process the voltage and current values is referred as the Incremental Conductance Algorithm (Wu 2003, Hua 2004). The central idea for this algorithm is based on the fact that the derivative of the output power P with respect to the

solar panel voltage V is equal to zero at the maximum power point. The algorithm checks the location of the present power point in relation to the maximum power point and will adjust the trim voltage. The trim voltage in turn adjusts the output voltage of SCBC to move the power point closer to the maximum (Cho 1999). The algorithm uses a search procedure based on current values and the voltage values. The maximum power is transferred when the incremental source impedance of the solar array matches with the load impedance. Figure 4 provides implementation details of the algorithm and explained in following paragraph. The term ($\Delta I/\Delta V$) in the flow chart in Figure 4 represents the incremental conductance of the source and (I/V), the load impedance. The search procedure in the flow chart finds the optimal operating point (I, V) where source impedance matches load impedance.

The current values of the voltage and current of the solar array are sampled and the values of ΔI and ΔV are computed. The search procedure initially moves the value of the boost value of the voltage by adjusting the trim voltage based on how source impedance matches with load impedance ($\Delta V < \varepsilon_1$). Once optimum boost voltage is obtained for the given power curve, optimum power curve is searched for until ($\Delta I < \varepsilon_3$).

3. IMPLEMENTATION AND CONCLUSION

The basic design of the peak power tracker will involve reading the voltage and current levels at the solar array output, processing these values using an algorithm, and then adjusting the voltage in order to obtain maximum power. The algorithm is implemented on a 68HC12 microcontroller. The microcontroller has an on-chip analog to digital controller that samples current values of voltage and current outputs of the solar array. An 8-bit value of the trim voltage is obtained from the algorithm. An AD7802, a digital to analog converter is interfaced to the microcontroller to generate the trim voltage. At present the design of the basic components of the project is completed. The design is at present being tested using a solar array simulator, Vicor DC-DC converter chip and a load bank, which will act as the satellite load. The results will be presented at the conference. The overall goal of the design is to ensure that the maximum power will be provided to the load at all times.

4. REFERENCES

[1]. Button, Robert M. "An Advanced Photovoltaic Array Regulator Module." *NASA Technical Memorandum*. August 1996.

[2]. Button, R., Iler T., and Liffring, M. A Modular, Peak Power Tracking Solar Array Regulator. *Proceedings of the 34th Intersociety Energy Conversion*

Engineering Conference (IECEC), **1999**, Vancouver, British Columbia, August 2-5, 1999.

[3]. Button, R. Electrical Systems Development Branch: Improved SCBC Controller. NASA Glenn Research Center. 27 Nov. 1995. <*http://powerweb.grc.nasa.gov/elecsys/doc/control.html*>

[4]. Cho B., and Huynh P. Design and Analysis of a Regulated Peak-Power Tracking System. *IEEE Transactions on Aerospace and Electronic Systems,* **35** (1999): 84-92.

[5]. Hua C., and Lin J. A Modified Tracking Algorithm for Maximum Power Tracking of Solar Array. *Energy Conversion and Management*, **45** (2004): 911-925.

[6]. Wu W., Pongratananukul N., Qiu W., Rustom K., Kasparis T., and Batarseh I., DSP-based Multiple Peak Power Tracking for Expandable Power System. *IEEE Power Electronics Specialists Conference*, **(2003):** 525-530.